

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. *(Previously Presented)* A method of testing the operation of an electronic unit by stimulating said unit with simulated input signals to said unit, the method comprising:

 processing at least one output signal from said unit at a first frequency in response to said simulated input signals;

 storing values of parameters corresponding to said processed signals; and

 accessing said stored parameter values at a second frequency which is slower than said first frequency and is compatible with an operating frequency of a microprocessor that generates said simulated input signals.
2. *(Original)* A method according to claim 1, wherein said parameter values are representative of switching instants of logic signals generated by said unit.
3. *(Original)* A method according to claim 2, wherein said parameter values are an image of said switching instants, of the duration during which a logic variable has a predetermined value, and/or the mean value of a logic variable over a predetermined period.

4. *(Cancelled)*.

5. *(Previously Presented)* An apparatus for testing the operation of an electronic unit by simulation, said unit generating logic signals at specific instants, said apparatus comprising:

a simulator which comprises at least one microprocessor sending input simulation signals to said unit and receiving output signals from said unit in response to said input simulation signals;

at least one programmable logic circuit which receives at least one of said output signals, said logic circuit generating, at a first frequency, parameter values corresponding to the signals received by said logic circuit; and

a storing circuit which stores said parameter values, wherein said microprocessor accesses said stored parameter values at a second frequency which slower than said first frequency and is compatible with an operating frequency of said microprocessor.

6. *(Previously Presented)* An apparatus according to claim 5 further comprising at least one second programmable logic circuit which sends in real time simulation signals to said unit on the basis of reference signals previously issued by said microprocessor.

7. (*Currently Amended*) An apparatus according to claim 6, wherein said programmable logic circuit which receives said at least one ~~some~~ of said output signals and said second programmable logic circuit which sends simulation signals to said unit are implemented as a single electronic circuit.

8. (*Previously Presented*) An apparatus according to claim 5, wherein at least one of said programmable logic circuit and said second programmable logic circuit is of the field programmable gate array type.

9. (*Previously Presented*) An apparatus according to claim 5, wherein said simulator further comprises at least one of:

an analog-to-digital converter which forward digital signals representative of analog signals generated by said unit to said microprocessor, and

a digital-to-analog converter which forwards analog simulation signals based on digital signals generated by said microprocessor to said unit.

10. (*Previously Presented*) An apparatus according to claim 5, wherein at least one of said programmable logic circuit and said second programmable logic circuit is programmed as a function of the type and/or intended use of said unit.

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. APPLICATION NO. 09/650,726
ATTORNEY DOCKET NO. Q60462

11. (*Cancelled*).